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**In the claims:**

Please amend the claims as follows:

1 (currently amended). A process for method of making a different types of various high-voltage bipolar/CMOS/DMOS (BCD) integrated circuits of different type using a limited number of different mask steps, said method comprising:

- (a) predefining a set of mask steps, each mask step comprising using a separate mask to perform an associated activity;
- (b) identifying a plurality of specific sequences of mask steps from said predefined set, each specific sequence being associated with the manufacture of one or more specific integrated circuits;
- (c) selecting a specific integrated circuit to manufacture;
- (d) selecting one of said specific sequences of mask steps from said predefined set of mask steps to manufacture said specific integrated circuit;
- a) providing a substrate or epitaxial layer of p-type material; and
- b) selecting a sequence of mask steps from a predefined set of mask steps (e) providing a substrate or epitaxial layer of p-type material; and
- (f) performing said selected sequence of mask steps in numerical order to make said selected specific integrated circuit; and
- said predefined set of mask steps selected from the group consisting of consisting essentially of:
  - (1) (1) applying a first mask a first step wherein a mask is used to form at least one N-well in said p-type material and forming at least one N-well in said p-type material therethrough;
  - (2) (2) applying a second mask and is used to forming an active region therethrough;
  - (3) a third step wherein a mask is used to (3) applying a third mask and forming a p-type field region therethrough;
  - (4) a fourth step wherein a (4) applying a fourth mask and is used to forming a gate oxide therethrough;
  - (5) (5) applying a fifth mask step wherein a mask is used to and carrying out a p-type implantation therethrough;

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(6) a sixth step wherein (6) applying a sixth mask and forming is used to form polysilicon gate regions therethrough;

(7) a seventh step wherein (7) applying a seventh a mask and forming is used to form a p-base region therethrough;

(8) an (8) applying an eighth mask step wherein a mask used to form and forming a N-extended region therethrough;

(9) (9) applying a ninth step wherein a -mask and is used to forming a p-top region therethrough;

(10) a tenth step wherein (10) applying a tenth mask and a mask is used to carrying out an N+ implant therethrough;

(11) an eleventh step wherein (11) applying an eleventh a mask and is used to carrying out a P+ implant therethrough;

(12) a(12) applying a twelfth mask step wherein a mask is used to and forming contacts therethrough;

(13) applying a thirteenth mask step wherein a mask is used in the and a deposition ofing a first metal layer therethrough;

(14) applying a fourteenth step wherein a mask and is used to forming vias in underlying material therethrough;

(15) applying a fifteenth mask step wherein a mask is used in the deposition of and depositing a second metal layer therethrough; and

(16) applying a sixteenth mask step wherein a mask is used in the formation of and forming a passivation layer therethrough; and

wherein said sequence consists of at least said mask steps 1 to 3, 5, 6, and 10 to 16 and at least one of said mask steps 4, 7, 8, and 9 depending on the type of integrated circuit; and

performing said selected sequence of mask steps in numerical order.

2.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprisesing mask steps 1, 2, 3, 5, 6, 8, 10, 11, 12, 13, 14, 15, and 16.

3.(currently amended) A processmethod as -claimed in claim 1, comprising wherein said selected sequence comprises mask steps 1, 2, 3, 5, 6, 9, 10, 11, 12, 13, 14, 15, and 16.

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4.(currently amended) A processmethod as claimed in claim 1, comprising wherein said selected sequence comprises mask steps 1, 2, 3, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

5.(currently amended) A processmethod as claimed in claim 1, comprising mask steps 1, 2, 3, 5, 6, 7, 10, 11, 12, 13, 14, 15, and 16.

6.(currently amended) A processmethod as claimed in claim 1, comprising wherein said selected sequence comprises mask steps 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, and 16.

7.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising-mask steps 1, 2, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15, and 16.

8.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising-mask steps 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

9.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising-mask steps 1, 2, 3, 4, 5, 6, 10, 11, 12, 13, 14, 15, and 16.

10.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising-mask steps 1, 2, 3, 4, 5, 6, 9, 10, 11, 12, 13, 14, 15, and 16.

11.(previously amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising-mask steps 1, 2, 3, 4, 5, 6, 8, 10, 11, 12, 13, 14, 15, and 16.

12.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising-mask steps 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

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13.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising mask steps 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

14.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising mask steps 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, and 16.

15.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising mask steps 1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, and 16.

16.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising mask steps 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, and 16.

17.(currently amended) A processmethod as claimed in claim 1, wherein said selected sequence comprises comprising mask steps 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

18(cancelled)

19(cancelled)

20.(previously added) A method as claimed in claim 1, wherein:

a) step 1 comprises the sub-steps of:

- (i) using P- bulk Silicon as a starting material;
- (ii) performing an initial oxidation;
- (iii) performing a photolithographic step;
- (iv) performing an N-Type Implant to create said N-Well; and
- (v) performing a diffusion;

b) step 2 comprises the sub-steps of:

- (i) performing an oxide etch;

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- (ii) performing an oxidation;
- (iii) performing a silicon nitride deposition;
- (iv) performing a photolithographic step; and
- (v) performing a nitride etch;

c) step 3 comprises the sub-steps of:

- (i) performing a photolithographic step;
- (ii) performing a P-Type Implant;
- (iii) performing a blanket N-Type Implant;
- (iv) performing an oxidation step to form a field oxide;
- (v) performing a nitride etch;
- (vi) performing an oxide etch; and
- (vii) performing an oxidation to form a pre-gate oxide;

d) step 4 comprises the sub-steps of:

- (i) performing an oxide etch;
- (ii) performing an oxidation the gate oxide; and
- (iii) performing a photolithographic step;

e) step 5 comprises the sub-steps of:

- (i) performing an oxide etch;
- (ii) performing an oxidation to form said thin gate oxide;
- (iii) performing a photolithographic step;
- (iv) performing a P-Type Implant;

f) step 6 comprises the sub-steps of:

- (i) performing polysilicon gate deposition;
- (ii) performing polysilicon doping;
- (iii) performing a photolithographic step;
- (iv) performing a polysilicon etch;

g) step 7 comprises the sub-steps of:

- (i) performing a photolithographic step;
- (ii) performing a P-type implant to form the P-base;

h) step 8 comprises the sub-steps of:

- (i) performing a photolithographic step;
- (ii) performing an N-type implant;

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- i) step 9 comprises the sub-steps of:
  - (i) performing a photolithographic step;
  - (ii) performing a P-type implant;
- (j) step 10 comprises the sub-steps of:
  - (i) performing an oxidation and diffusion step;
  - (ii) performing a polysilicon oxidation;
  - (iii) performing a photolithographic step; and
  - (iv) performing an N-type implant to create said N<sup>+</sup> implant region;
- (k) step 11 comprises the sub-steps of:
  - (i) performing a photolithographic step; and
  - (ii) performing a P-type implant to create said P<sup>+</sup> implant region;
- (l) step 12 comprises the sub-steps of:
  - (i) performing a SG/PSG/SOG deposition;
  - (ii) performing a diffusion step; and
  - (iii) performing a photolithographic step; and
  - (iv) performing a contact etch;
- (m) step 13 comprises the sub-steps of:
  - (i) performing a Ti/TiN deposition with oxidation;
  - (ii) performing an aluminum alloy deposition;
  - (iii) performing a photolithographic step;
  - (iv) performing a metal etch; and
  - (v) performing dielectric and SOG deposition;
- (n) step 14 comprises the sub-steps of:
  - (i) performing a photolithographic step; and
  - (ii) etching said vias; and
- (o) step 15 comprises the sub-steps of:
  - (i) performing Ti/TiN deposition with oxidation;
  - (ii) performing an aluminum alloy deposition;
  - (iii) performing a photolithographic step;
  - (iv) performing a metal etch;
  - (v) performing an oxide/nitride deposition;

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- (vi) performing a photolithographic step; and
- (vii) performing an oxide etch.